Amendments to the Specification:

Page 32, line 31 through page 33, line 18, please amend the paragraph as follows:

Fractional bits a_5-a_0 1511-1516 are compared in comparator 1520 with the preselected threshold value f_t 1522, which value is maintained in a storage device (not shown) ~~1524~~. Where it is desired to implement a sign-bit rounding technique, similar to one discussed relative to method 800 and FIG. 8, the value of sign bit s_i 1530 is selected by MUX 1532 to be combined with the precision portion 1534 of the output of comparator 1520, which constitutes the rounding operand. If the sign-bit technique is selected by bias control 1550, then when input signal X 1510 has positive polarity, then the value of binary '0' becomes selectable bias α 1533 which is combined with bit a_3 1513. On the other hand, when input signal X 1510 has negative polarity, then the value of binary '1' becomes selectable bias α 1533 which is combined with bit a_3 1513. If the current rounding state is not the threshold rounding state, then bit a_2 1514, can be selectively added to bit a_3 1513 under the direction of bias controller 1550, in a manner consistent with the rounding technique chosen (e.g., RTZ, RTN, RTC, RTF, and RTE). Adder 1535 is designed with a seven-bit input and seven bit output, thus inherently dropping loss bits a_2-a_0 (1514-1516), and producing signed output signal 1545 with 3 bit fractional portion b_2-b_0 1548.